

# DATA SHEET

## **SA7026**

1.3GHz low voltage fractional-N dual  
frequency synthesizer

Objective specification  
Supersedes data of 1998 Apr 06

1998 Oct 13

# 1.3GHz low voltage fractional-N dual synthesizer

# SA7026

## FEATURES

- Low phase noise
- Low power
- Fully programmable main and auxiliary dividers
- NORMAL & INTEGRAL charge pumps outputs
- Fast Locking Adaptive mode design
- Internal fractional spurious compensation
- Hardware and software power down

## APPLICATIONS

- 500–1300 MHz wireless equipment
- Cellular phones
- Portable battery-powered radio equipment.

## General description

The SA7026 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 1.3 GHz. The synthesizer has fully programmable main, auxiliary and

reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage.  $V_{DDCP}$  could be greater than or equal to  $V_{DD}$ .

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin ). Only passive loop filters are used; the charge-pump operates within a wide voltage compliance range to provide a wider tuning range.

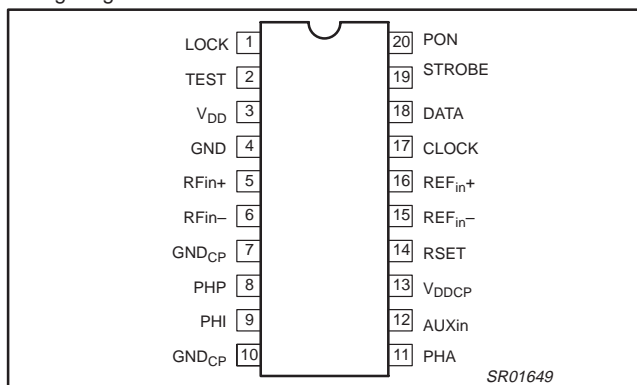


Figure 1. Pin Configuration

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Supply voltage	V <sub>DD</sub>	2.7	–	5.5	V
V <sub>DDCP</sub>	Analog supply voltage	V <sub>DDCP</sub> ≥ V <sub>DD</sub>	2.7	–	5.5	V
I <sub>DDCP</sub> +I <sub>DD</sub>	Supply current	Main and Aux. on	–	7.5	8.8	mA
I <sub>DDCP</sub> +I <sub>DD</sub>	Total supply current in power-down mode		–	1	–	μA
f <sub>VCO</sub>	Input frequency		500	–	1300	MHz
f <sub>AUX</sub>	Input frequency		10	–	550	MHz
f <sub>REF</sub>	Crystal reference input frequency		10	–	40	MHz
f <sub>PC</sub>	Maximum phase comparator frequency		–		4	MHz
T <sub>amb</sub>	Operating ambient temperature		–40	–	+85	°C

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		VERSION
	NAME	DESCRIPTION	
SA7026DK	TSSOP20	Plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360–1

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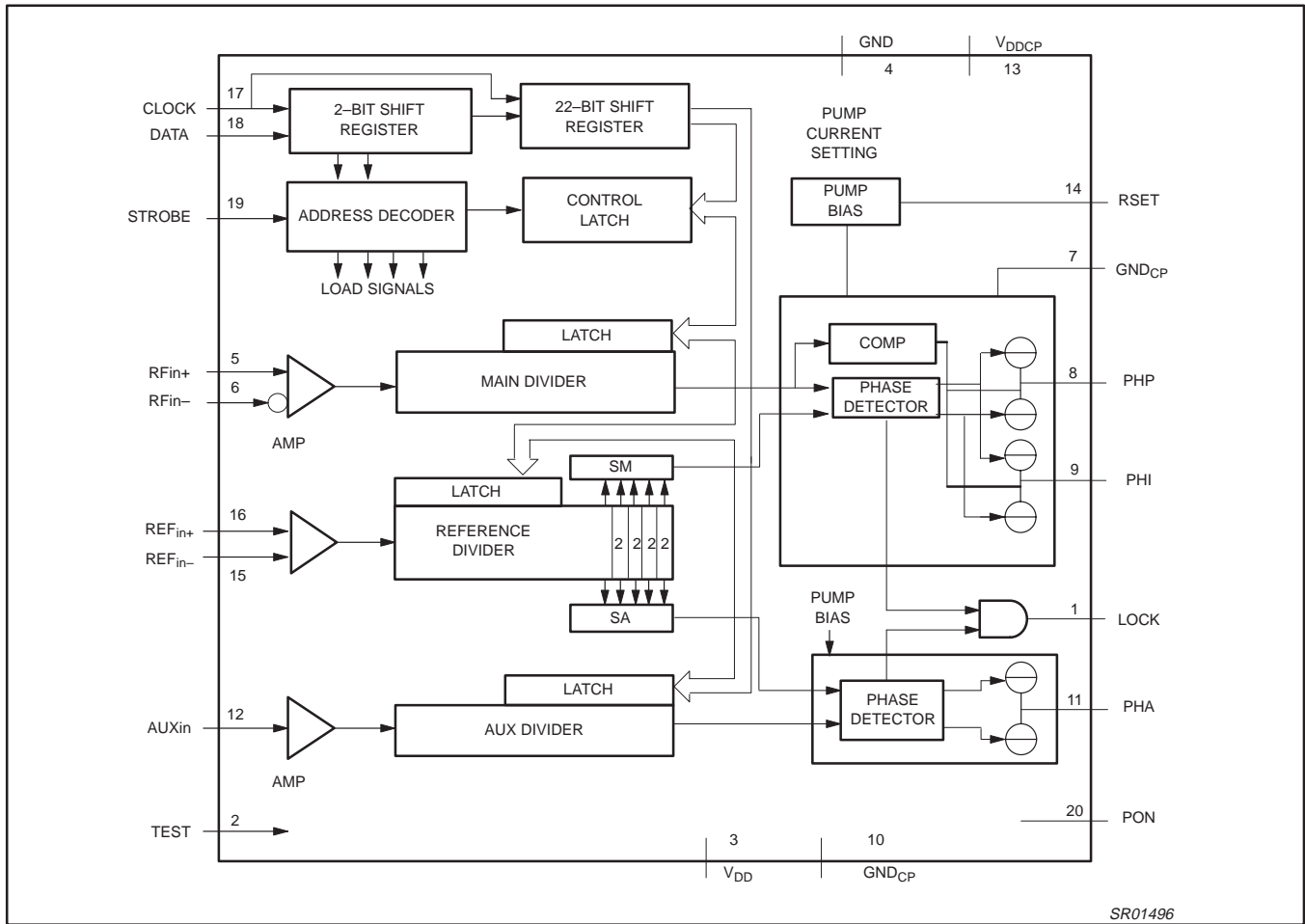


Figure 2. Block Diagram

## PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V <sub>DD</sub>	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin-	6	RF negative input to main divider
GND <sub>CP</sub>	7	Charge pump ground
PHP	8	Main NORMAL chargepump
PHI	9	Main INTEGRAL chargepump
GND <sub>CP</sub>	10	Charge Pump Ground

SYMBOL	PIN	DESCRIPTION
PHA	11	Auxiliary chargepump output
AUXin	12	Input to auxiliary divider
V <sub>D<sub>DCP</sub></sub>	13	Charge pump supply voltage
RSET	14	External resistor from this pin to ground sets the chargepump current
REF <sub>in-</sub>	15	Reference input
REF <sub>in+</sub>	16	Reference input
CLOCK	17	Programming bus clock input
DATA	18	Programming bus data input
STROBE	19	Programming bus enable input
PON	20	Power down control

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**Characteristics** $V_{DDCP} = V_{DD} = +3.0V$ ,  $T_{amb} = +25^{\circ}C$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply; pins 3, 13</b>						
$V_{DD}$	Digital supply voltage		2.7	–	5.5	V
$V_{DDCP}$	Analog supply voltage	$V_{DDCP} = V_{DD}$	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	$V_{DD} = +3.0V$ (with main and aux on)	–	7.5	8.8	mA
$I_{standby}$	Total supply current in power-down mode	logic levels 0 or $V_{DD}$	–	1	TBD	$\mu A$
<b>RFin main divider input; pins 5, 6</b>						
$f_{VCO}$	VCO input frequency		500	–	1300	MHz
$V_{RFin(rms)}$	AC-coupled input signal level	$R_s = 50\Omega$ ; MAX. limit is indicative	–18	–	0	dBm
$Z_{IRFin}$	Input impedance (real part)	$f_{VCO} = 2.0\text{ GHz}$	–	TBD	–	$k\Omega$
$C_{IRFin}$	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
$N_m$	Main divider ratio		512	–	65535	
$f_{PCmax}$	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
<b>AUX reference divider input; pins 12</b>						
$f_{AUXin}$	Input frequency range		10	–	550	MHz
$V_{AUXin}$	AC-coupled input signal level	$R_s = 50\Omega$ ; MAX. limit is indicative	–18	–	0	dBm
			80	–	636	mVpp
$Z_{AUXin}$	Input impedance (real part)	$f_{VCO} = 500\text{ MHz}$	–	TBD	–	$k\Omega$
$C_{AUXin}$	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
$N_{AUX}$	Auxiliary division ratio		128	–	16384	
<b>Reference divider input; pins 15, 16</b>						
$f_{REFin}$	Input frequency range from crystal		10	–	40	MHz
$V_{RFin}$	AC-coupled input signal level	$R_s = 50\Omega$ ; MAX. limit is indicative	360	–	1300	mVpp
$Z_{REFin}$	Input impedance (real part)		–	TBD	–	$k\Omega$
$C_{REFin}$	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
$R_{REF}$	Reference division ratio	SA=SM="000"	4	–	1023	
<b>Charge pump current setting resistor input; pin 14</b>						
$R_{SET}$	External resistor from pin 3 to ground		6	7.5	24	$k\Omega$
$V_{SET}$	Regulated voltage at pin 3	$R_{SET} = 7.5\text{ k}\Omega$	–	1.25	–	V
<b>Charge pump outputs (including fractional compensation pump); pins 8, 9, 11; <math>R_{SET} = 7.5\text{ k}\Omega</math>, <math>FC = 80</math></b>						
$I_{cp}$	Chargepump current ratio to $I_{set}$	CURRENT GAIN $I_{PH}/I_{SET}$	–15		+15	%
$I_{MATCH}$	Sink-to-source current matching	$V_{ph} = 1/2 V_{DDCP}$	–10		+10	%
$I_{ZOUT}$	Output current variation versus $V_{ph}^2$	$V_{ph}$ in compliance range	–10		+10	%
$I_{LPH}$	Charge pump off leakage current	$V_{cp} = 1/2 V_{CC}$	–10		+10	nA
$V_{ph}$	Charge pump voltage compliance		0.7	–	$V_{DDCP} - 0.8$	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Phase noise</b>						
C/N	Synthesizer's contribution to close-in-phase noise of 1300 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=240kHz indicative, not tested	-	-77	-	$\frac{\text{dBc}}{\text{Hz}}$
<b>Interface logic input signal levels; pins 3, 15, 16, 18, 19, 20</b>						
V <sub>IH</sub>	HIGH level input voltage		0.7*V <sub>DD</sub>	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	LOW level input voltage		-0.3	-	0.3*V <sub>DD</sub>	V
I <sub>bias</sub>	Input bias current	logic 1 or logic 0	-5	-	+5	$\mu\text{A}$
<b>Lock detect output signal (in push/pull mode); pin 1</b>						
V <sub>OL</sub>	LOW level output voltage	I <sub>sink</sub> = 2mA	-	-	0.4	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>source</sub> = -2mA	V <sub>DD</sub> -0.4	-	-	V

**NOTES:**

1.  $I_{SET} = \frac{V_{SET}}{R_{SET}}$  bias current for charge pumps.

2. The relative output current variation is defined thus:

$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{I_1(I_2 + I_1)}; \text{ with } V_1 = 0.7V, V_2 = V_{DDCP} - 0.8V \text{ (See Figure 3.)}$$

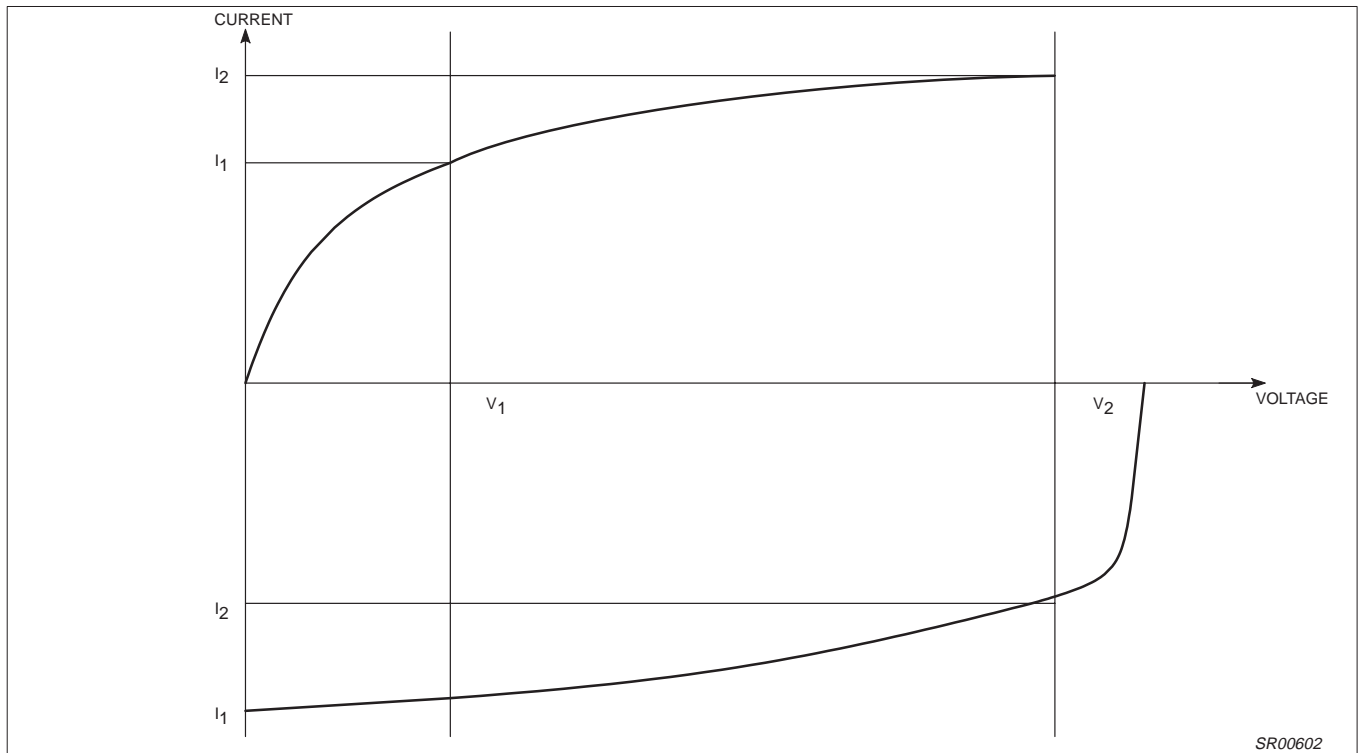


Figure 3. Relative Output Current Variation

SR00602

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD}$	Digital supply voltage	-0.3	+5.5	V
$V_{DDCP}$	Analog supply voltage	-0.3	+5.5	V
$\Delta V_{DDCP-V_{DD}}$	Difference in voltage between $V_{DDCP}$ and $V_{DD}$ ( $V_{DDCP} \geq V_{DD}$ )	-0.3	+2.8	V
$V_n$	Voltage at pins 1, 2, 5, 6, 12, 15 to 20	-0.3	$V_{DD} + 0.3$	V
$V_1$	Voltage at pin 8, 9, 13	-0.3	$V_{DDCP} + 0.3$	V
$\Delta V_{GND}$	Difference in voltage between $GND_{CP}$ and $GND$ (these pins should be connected together)	-0.3	+0.3	V
$P_{tot}$	Total power dissipation		TBD	mW
$T_{stg}$	Storage temperature	-55	+125	°C
$T_{amb}$	Operating ambient temperature	-30	+85	°C
$T_j$	Maximum junction temperature		TBD	°C

**Handling**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	Thermal resistance from junction to ambient in free air	120	K/W

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## FUNCTIONAL DESCRIPTION

### Main Fractional-N divider

The RFin input (pins 5 and 6) drive a pre-amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from -18dBm to +0dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Divide ratios (512 to 65536) allow a minimum phase comparison frequency of 25kHz at 2.5 GHz RF.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$N_{frac} = N + \frac{NF}{Q}$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new programming word is synchronized to the state of the main divider to avoid introducing a phase disturbance.

### Auxiliary divider

The auxiliary divider consists of a divider with fully programmable values between 128 and 16384. The AUXin input, pin 13, drives a pre-amplifier to provide the clock to the first divider stage. The AUXin negative input is internally connected to ground. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from -18dBm to +0dBm (80 to 636 mVpp), and at frequencies as high as 550 MHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. The divide ratios allow a minimum phase comparison frequency of 25kHz at 550 MHz RF.

### Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3 bit SM (SA) register (see figure 4) determines which of the 5 output pulses are selected as the main (auxiliary) phase detector input.

### Phase detector

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by an external resistor. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

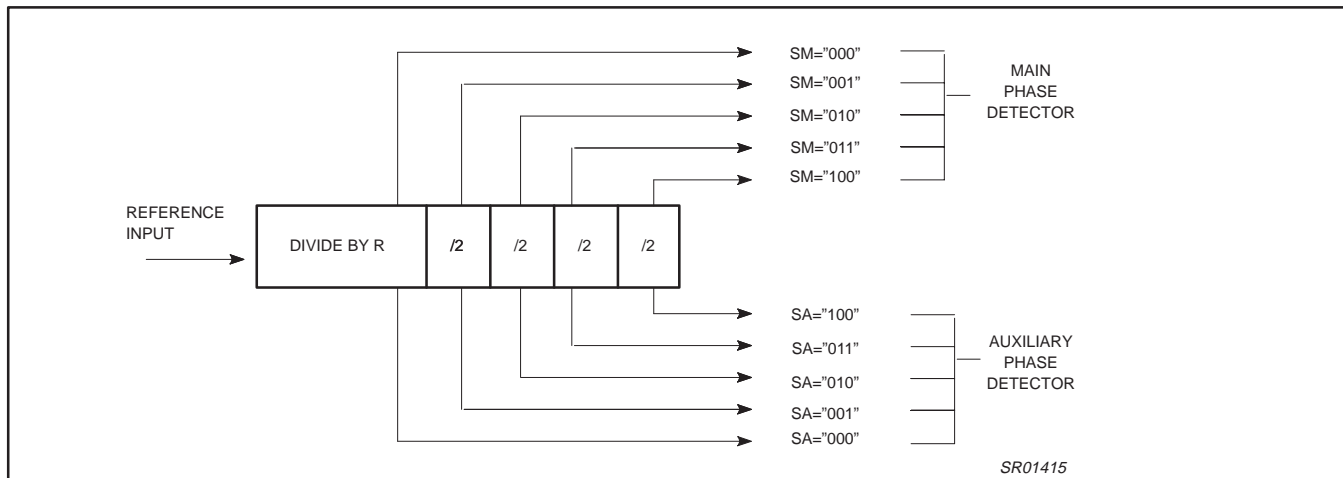


Figure 4. Reference Divider

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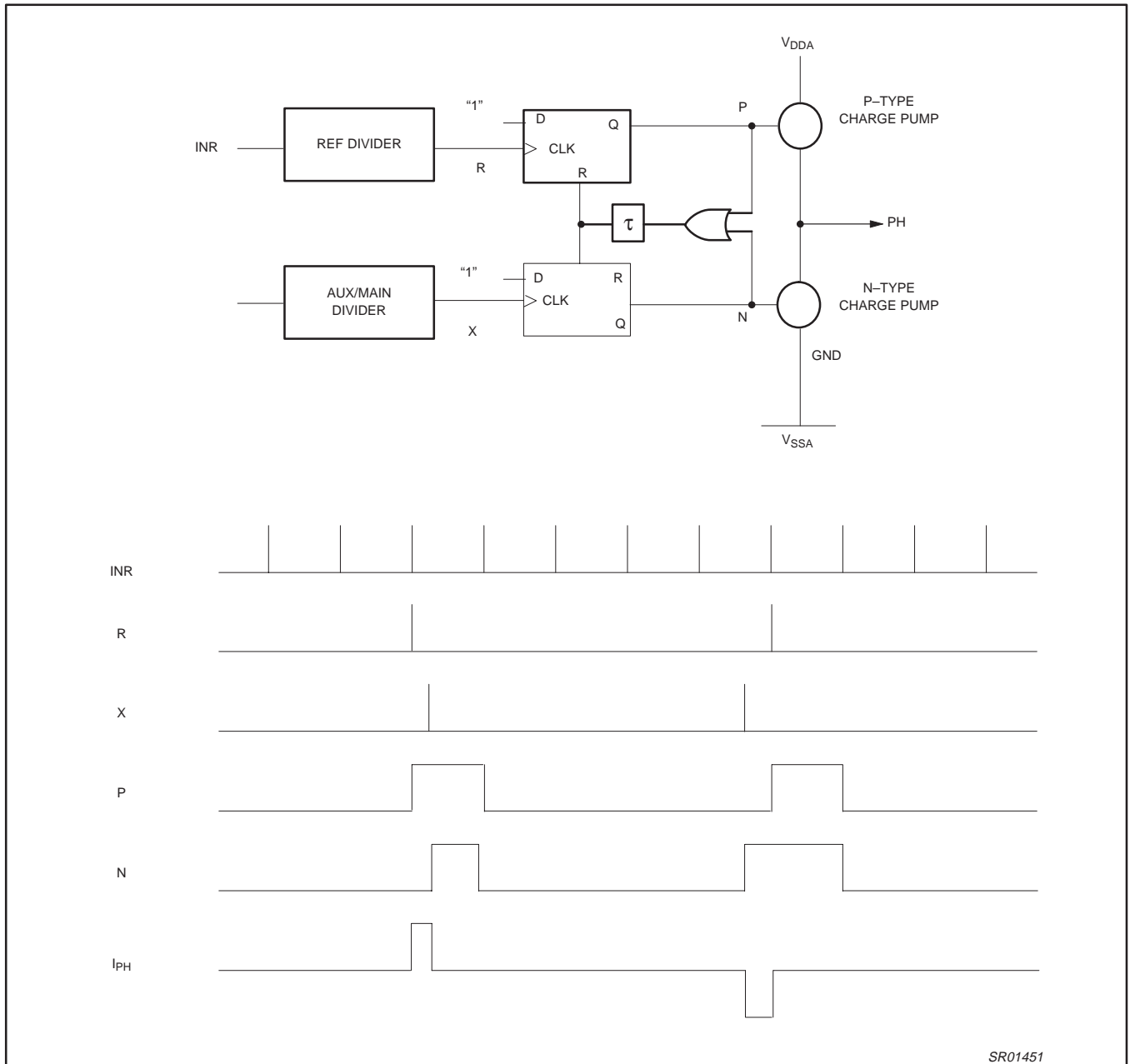


Figure 5. Phase Detector Struction with Timing

SR01451



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## Main Output Charge Pumps and Fractional Compensation Currents.

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin RSET. The fractional compensation is derived from the current at RSET, the contents of the fractional accumulator FRD and by the program value of the FDAC. The timing for the fractional compensation is derived from the main divider. See table of charge pump ratios.

## Principle of Fractional Compensation

The fractional compensation is designed into the circuit as a means of reducing or eliminating fractional spurs that predominate when the accumulator rolls over and the main divider counts one extra RF input cycle (+1, swallows a cycle). Since  $I_{COMP}$  is the compensation current and  $I_{PUMP}$  is the pump current, for each charge pump,

$$I_{PUMP\_TOTAL} = I_{PUMP} + I_{COMP}$$

The theoretical values for FDAC are: 128 for FMOD = 1 (modulo 5) and 80 for FMOD = 0 (modulo 8). Fractional division will cause the pump to output a charge that is compensated for in order to reduce fractional spurs. This compensation is done by sourcing a small current,  $i_A$ , see Figure 7, that is proportional to the fractional error phase. Figure 6 shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple.

This means  $I_{PUMP} * Q = I_{COMP} * 128$ , where Q equals fractional-N modulus e.g., 2/5 for NF = 2 and FMOD = 1. The fractional compensation current is derived from the main charge pump in that it follows all the current scaling through external resistor setting, RN, programming or speed-up operation. For a given pump,

$$I_{COMP} = ( I_{PUMP} / 128 ) * ( FDAC / 5 * 128 ) * FRD$$

FRD is the fractional accumulator value.

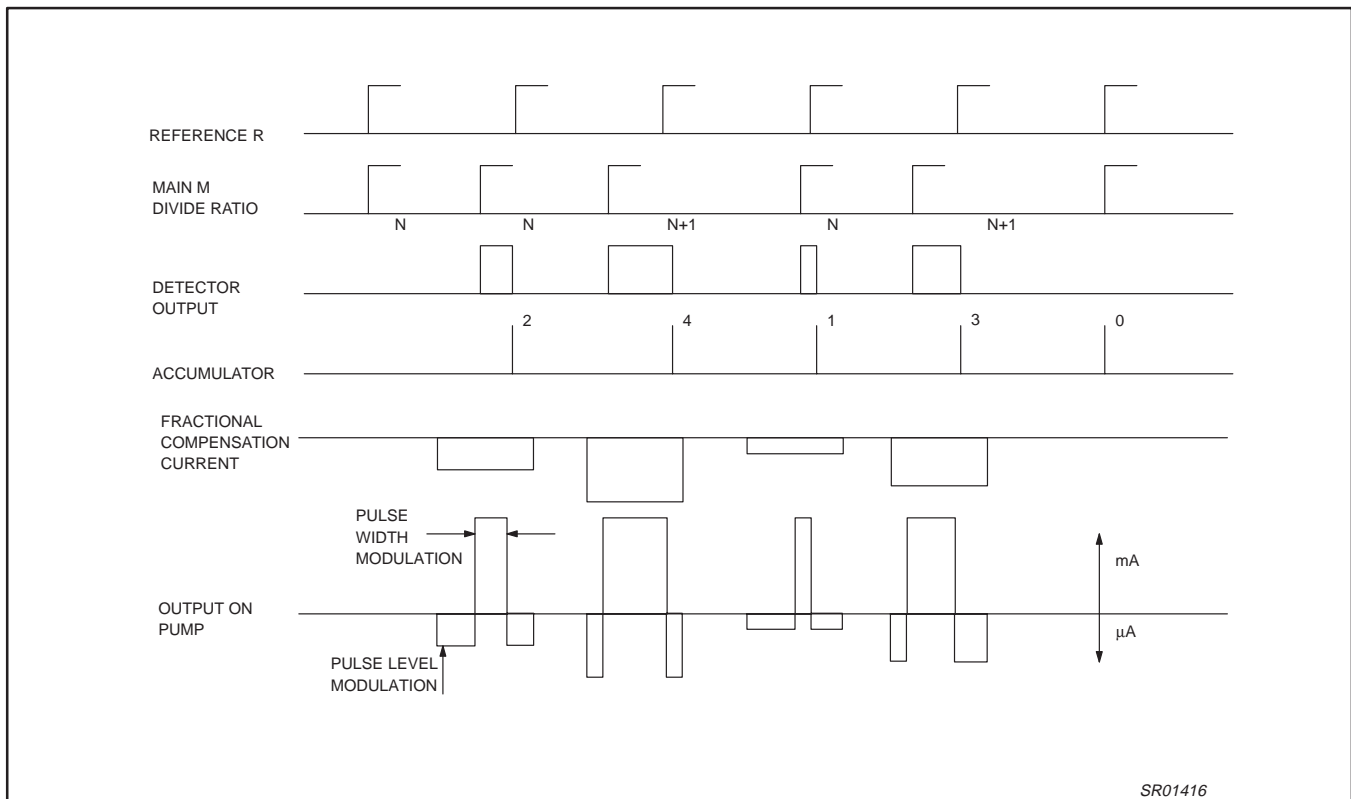


Figure 6. Waveforms for NF = 2, Fraction = 0.4

Fig 6. shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

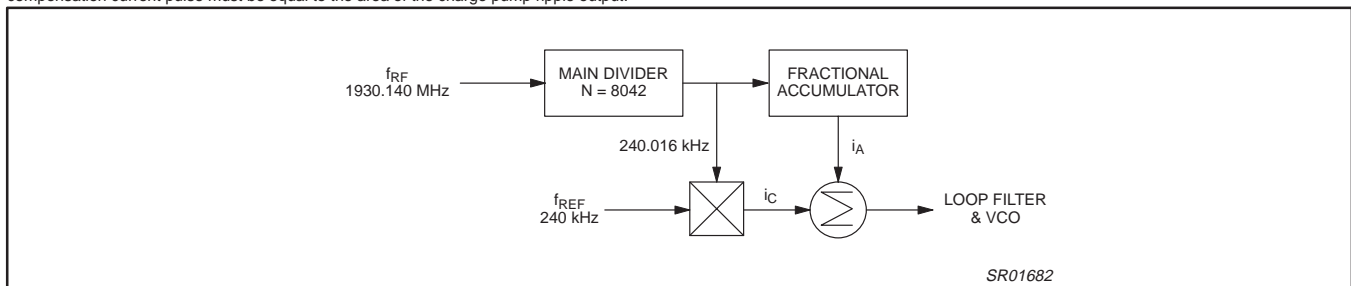


Figure 7. Current Injection Concept

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**Auxiliary Output Charge Pumps**

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor attached to pin R<sub>set</sub>.

**Main and auxiliary chargepump currents**

CP1	CP0	I <sub>PHA</sub>	I <sub>PHP</sub>	I <sub>PHP-SU</sub>	I <sub>PHI</sub>
0	0	1.5xI <sub>set</sub>	3xI <sub>set</sub>	15xI <sub>set</sub>	36xI <sub>set</sub>
0	1	0.5xI <sub>set</sub>	1xI <sub>set</sub>	5xI <sub>set</sub>	12xI <sub>set</sub>
1	0	1.5xI <sub>set</sub>	3xI <sub>set</sub>	15xI <sub>set</sub>	0
1	1	0.5xI <sub>set</sub>	1xI <sub>set</sub>	5xI <sub>set</sub>	0

**NOTES**

1.  $I_{SET} = V_{set}/R_{set}$ : bias current for charge pumps.
2. CP1 is used to disable the PHI pump, I<sub>PHP-SU</sub> is the total current at pin PHP during speed up condition.

**Lock Detect**

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than  $\pm 1$  period of the frequency at the input REF<sub>in+</sub>, -. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic '0') is indicated when both counters are powered down.

**Power-down mode**

The power-down signal can be either hardware (PON) or software (PD). The PON signal is exclusively ORed with the PD bits. If PON = 0, then the part is powered up when PD = 1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after the power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

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### Serial programming bus

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. The programming data is structured into 24 bit words; each word includes 2 address bits. Figure 8 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the 2 address bits the data is latched into

different working registers or temporary registers. In order to fully program the synthesizer, 3 words must be sent: C, B, and A. Table 1 shows the format and the contents of each word. The D word is for testing purposes only. The data for the fractional compensation DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

### Serial bus timing characteristics. See Figure 8.

$V_{DD} = V_{DDCP} = +3.0V$ ;  $T_{amb} = +25^{\circ}C$  unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
<b>Serial programming clock; CLK</b>					
$t_r$	Input rise time	–	10	40	ns
$t_f$	Input fall time	–	10	40	ns
$T_{cy}$	Clock period	100	–	–	ns
<b>Enable programming; STROBE</b>					
$t_{START}$	Delay to rising clock edge	40	–	–	ns
$t_w$	Minimum inactive pulse width	$1/f_{comp}$	–	–	ns
$T_{SU;\bar{E}}$	Enable set-up time to next clock edge	20	–	–	ns
<b>Register serial input data; DATA</b>					
$t_{SU;DAT}$	Input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

### Application information

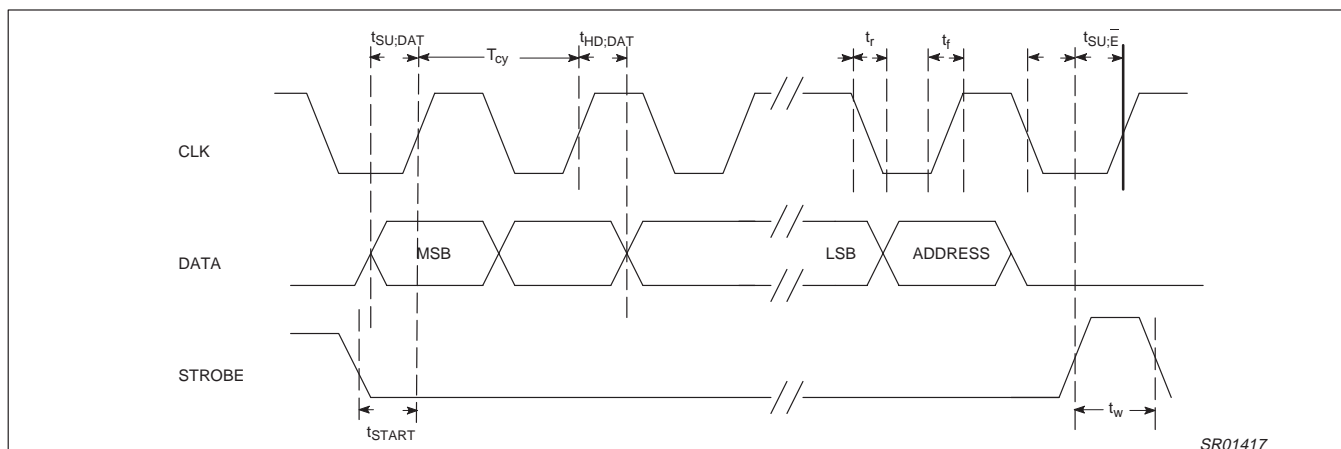


Figure 8. Serial Bus Timing Diagram

SR01417

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## Data format

**Table 1. Format of programmed data**

LAST IN				MSB		SERIAL PROGRAMMING FORMAT						FIRST IN LSB	
p23		p22		p21		p20	../..	../..			p1		p0

**Table 2. A word, length 24 bits**

LAST IN						MSB																LSB		FIRST IN	
Address		fmod	Fractional-N			Main Divider ratio														Spare					
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SK1	SK2		
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0		
A word select				Fixed to 00.																					
Fractional Modulus select				FM 0 = modulo 8, 1 = modulo 5.																					
Fractional-N Increment				NF2..0 Fractional N Increment values 000 to 111.																					
N-Divider				N0..N15, Main divider values 512 to 65535 allowed for divider ratio.																					

**Table 3. B word, length 24 bits**

ADDRESS		REFERENCE DIVIDER									LOCK		PD		FRACTIONAL COMPENSATION DAC									
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	L1	L0	Main	Aux	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	
Default:		0	0	0	1	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0
B word select				Fixed to 01																				
R-Divider				R0..R9, Reference divider values 4 to 1023 allowed for divider ration.																				
Lock detect output				L1 L0 00 Combined main, aux. lock detect signal present at the LOCK pin (push/pull). 01 Combined main, aux, lock detect signal present at the LOCK pin (open drain). 10 Main lock detect signal present at the LOCK pin. 11 Auxiliary loop lock detect signal present at the LOCK pin. When auxiliary loop and main loop are in power down mode, the lock indicator is low.																				
Power down				Main = 1: power to N-divider, reference divider, main charge pumps, Main = 0 to power down. Aux = 1: power to Aux divider, reference divider, aux charge pump, Aux = 0 to power down.																				
Fractional Compensation				FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255. Recommended values: FC = 80 for MOD 8; FC = 128 for MOD 5.																				

**Table 4. C word, length 24 bits**

Address		Auxiliary Divider										CP		SM			SA						
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	SM2	SM1	SM0	SA2	SA1	SA0
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0
C word select				Fixed to 10																			
A-Divider				A0..A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.																			
Charge pump current Ratio				CP1, CP0: Charge pump current ratio, see table of charge pump currents.																			
Main comparison select				SM comparison divider select for main phase detector.																			
Aux comparison select				SA Comparison divider select for auxiliary phase detector.																			

**Table 5. D word, length 24 bits**

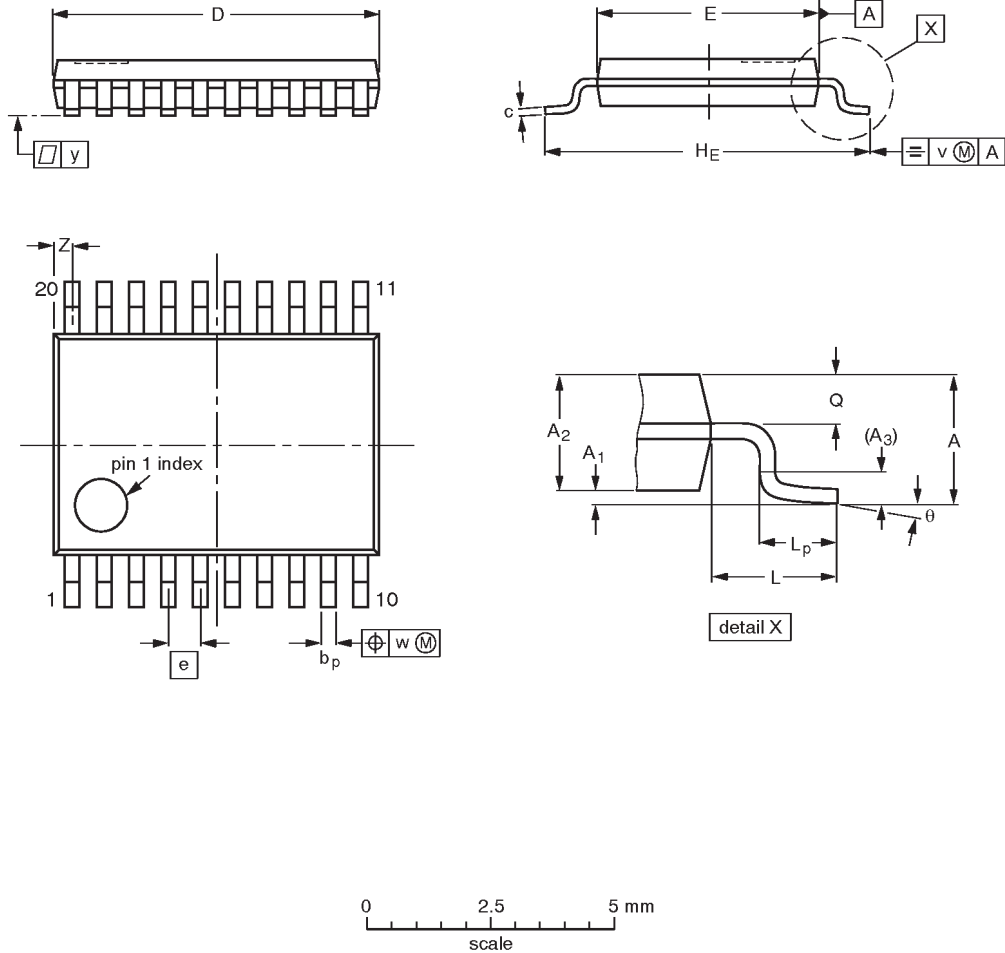
ADDRESS			SYNTHESIZER TEST BITS				SYNTHESIZER TEST BITS																
1	1	0	-	-	-	-	T <sub>spu</sub>	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DEFAULT			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T <sub>spu</sub> : Speed up							Forces the synthesizer charge pump in speed-up mode all the time. <b>NOTE:</b> All test bits must be set to 0 for normal operation.																

# 1.3GHz low voltage dual fractional-N frequency synthesizer

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

# 1.3GHz low voltage dual fractional-N frequency synthesizer

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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